

Attorney Docket No.: 42P7794

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Anand Murthy, et al.

Application No. 09/475,452

Filed: 12/30/1999

For: A NOVEL MOS TRANSISTOR
STRUCTURE AND METHOD OF
FABRICATION

Examiner: Lee, Eugene

Art Unit: 2815

Mail Stop Amendments
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450DECLARATION UNDER 37 C.F.R. § 1.132

I, Anand Murthy, do hereby declare and say:

My home address is 10934 NW Lucerne Ct., Portland OR 97229.

I have a Master of Science degree in Welding Engineering from Ohio State University, and a Doctoral degree in Material Science from the University of Southern California.

I am presently employed by Intel Corporation, as a senior Engineering Manager in Logic Technology Development. I lead an engineering team to develop advanced strained transistors based on novel epitaxial deposition for 32nm node and beyond. I was responsible for introducing industry-leading first-ever strained PMOS transistors using embedded SiGe for the 90nm technology node. I subsequently led the development of strain enhancement in PMOS transistors in 65 and 45nm generation nodes. I am recipient of two Intel Achievement

(IAA) awards, have co-authored in over 50 technical publications and hold 28 U.S. Patents, the majority of them granted for pioneering work in epitaxial deposition to enable strained transistors. I have been with Intel since 1995.

I am one of the inventors in the above referenced application. I have reviewed the application. I have also reviewed a copy of the pending claims set forth in Exhibit A that include amendments made by an Amendment accompanying my Declaration.

I have been given a copy of U.S. Patent No. 5,060,033 to Takeuchi et al. (" '033 patent") and I have carefully studied it. I am familiar with and fully understand the disclosure of the '033 patent.

The '033 patent discloses a MOS transistor that comprises a semiconductor substrate 101, an insulation film 102 on the substrate 101, a p-type layer 104 on the semiconductor substrate 101, a gate electrode 105, source drain regions 106 and 109 (Figure 1h, col. 3, lines 49-65).

The '033 patent discloses forming source and drain regions by ion implantation of the impurities at opposing sides of gate electrode (Figure 1(e), col. 4, lines 37-44). It is well known in the art that the ion implantation causes strong diffusion of the dopants into the substrate. Such strong diffusion causes the dopant concentration to transit gradually from source/drain regions into the substrate resulting in a smooth junction. Accordingly, the ion implantation technique used in '033 patent cannot provide source and drain regions having an abrupt junction. A MOS transistor of the subject application, in contrast, relies on the following key feature: the inwardly concaved recesses with the inflection points in the substrate backfilled with insitu doped semiconductor material that provide source and drain regions with extensions having an abrupt junction. Such source/drain regions with extensions having an abrupt junction are not achievable by ion implantation techniques.

Exhibit B includes photocopies of the experimental graphs (Figures 1 and 2). Figure 1 shows the secondary ion mass spectrometry ("SIMS") profile of the dopant concentration through the source/drain regions with source/drain extensions (tips) fabricated by backfilling the inwardly concaved recesses with the inflection points ("EPI-TIP"). Figure 2 shows the SIMS profiles of the dopant concentration for the source/drain regions fabricated by ion implantation ("As Implanted"). As shown in Figure 2, the ion implantation with or without annealing provides a substantially smooth profile of the dopant concentration (more than 8nm/decade of the concentration change) that forms source/drain junction. As shown in the Figure 1, "epi-tip" fabrication, unlike ion implantation, provides an abrupt profile of the dopant concentration (less than 3.2 nm/decade of the concentration change) that forms an abrupt source/drain tip junction. The substantially sharper profile of the dopant concentration forms an abrupt source/drain junction between the first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the material of the first conductivity type region of the substrate, as claimed in the subject patent application. Such an abrupt junction (less than 3.2nm/decade of the concentration change) is not currently achievable by ion implantation and annealing techniques. Accordingly, the transistor taught by the '033 patent does not exhibit abrupt source/drain tip junction, as claimed in the subject patent application.

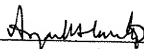
Based on these observations, it is my professional opinion that one of ordinary skill in the art at the time the invention was made, would not understand the '033 patent to suggest a pair of inwardly concaved source/drain regions with extensions at the inflection points having an abrupt junction (boundary) between the material of first silicon or silicon alloy layer filling the inwardly concaved recesses at the inflection points and the material of the first conductivity type region, as claimed in the subject patent application.

I have read the Amendment and Response to Final Office Action mailed on June 8, 2007 and agree with the statements made therein.

I declare, to the best of my knowledge, that all statements made in this document are true, and that all statements made on the information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-identified patent application or any patent issued thereon.

Signed

Date: 10/31/2007



Anand Murthy